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LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the claims of the present patent application.

1. (Currently Amended) A system for effectuating the transfer of data blocks having intervals across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

a first circuit portion for providing said data blocks to a second circuit portion;

a synchronizer controller disposed between said first and second clock domains for providing at least one dead cycle control signal to said second circuit portion, wherein said at least one dead cycle control signal is indicative of the location of at least one dead cycle between said first and second clock signal; and

control logic associated with said second circuit portion for generating data transfer control signals responsive to said at least one dead cycle control signal, said data transfer control signals for controlling said second circuit portion whereby said data blocks are transmitted as contiguous data blocks relative to said at least one dead cycle, wherein said control logic is operable to generate data transfer control signals for transferring multi-channeled packet data, each channel's data blocks being interleaved with data blocks of other channels.

2. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein said first circuit portion comprises a packet interface.

3. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein said second circuit portion comprises:

at least one queue operably coupled to said first circuit portion for temporarily storing said data blocks; and

a multiplexer (MUX) block operably coupled to said first circuit portion and said at least one queue, said MUX block operating under a MUX selection control signal generated by said control logic for selecting between data blocks stored in said at least one queue and data blocks provided by said first circuit portion without queuing, whereby said data blocks are transmitted as an output of said MUX block to a synchronizer operating under control of said synchronizer controller.

4. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein each of said data blocks comprises one bit.

5. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein each of said data blocks comprises multiple bits.

6. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein said data blocks comprise a header that provides protocol control information relative to said data blocks.

7. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 6, wherein said header is removed from said header blocks for processing by said control logic.

Claim 8 is cancelled.

9. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein said at least one dead cycle comprises N - M dead cycles.

10. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein at least one of said data blocks is positioned adjacent to said at least one dead cycle.

11. (Original) The system for effectuating the transfer of data blocks having intervals as recited in claim 1, wherein said dead cycle control signal is provided 0 to N - 1 cycles prior to said dead cycle.

12. (Currently Amended) A circuit for effectuating the transfer of data blocks ~~having intervals~~ to a synchronizer disposed between two clock domains, comprising:

means for receiving and temporarily storing a first portion of said data blocks having intervals; and

means for selecting between said first portion of said data blocks ~~stored in said means for receiving and temporarily storing~~ and a second portion of said data blocks having intervals provided without queuing, whereby said data blocks are transmitted to said synchronizer as a packet of contiguous data blocks relative to at least one dead cycle.

13. (Original) The circuit for effectuating the transfer of data blocks as recited in claim 12, wherein said means for receiving and temporarily storing a portion of said data blocks comprises at least one queue.

14. (Original) The circuit for effectuating the transfer of data blocks as recited in claim 12, wherein said means for receiving and temporarily storing a portion of said data blocks comprises at least one first-in-first-out (FIFO) queue.

15. (Currently Amended) The circuit for effectuating the transfer of data blocks as recited in claim 12, wherein said means for selecting between said ~~portion~~ first and second portions of said data blocks comprises a multiplexer (MUX) block.

16. (Original) The circuit for effectuating the transfer of data blocks as recited in claim 12, further comprising means for signaling the location of at least one dead cycle relative to said two clock domains.

17. (Currently Amended) The circuit for effectuating the transfer of data blocks as recited in claim 12, wherein said means for selecting between said ~~portion~~ first and second portions of said data blocks is coupled to said synchronizer operable to transfer said data blocks from a fast clock domain to a slow clock domain.

18. (Currently Amended) The circuit for effectuating the transfer of data blocks as recited in claim 12, wherein said means for selecting between said ~~portion~~ first and second portions of said data blocks is coupled to said synchronizer operable to transfer said data blocks from a core clock domain to a bus clock domain.

19. (Currently Amended) A method for effectuating the transfer of data blocks having intervals across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second clock signal (CLK2), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

generating advance notice indicative of the location of at least one dead cycle occurring between a first clock signal and a second clock signal used for transmitting data across a clock boundary;

receiving packet data and said advance notice indicative of the location of said at least one dead cycle, said packet data including said data blocks having intervals;

calculating the optimal time to send said packet data relative to the location of said at least one dead cycle; and

transmitting ordered contiguous data blocks about said at least one dead cycle to a CLK1-to-CLK2 synchronizer for

transmission to receive circuitry disposed in said second clock domain.

20. (Original) The method for effectuating the transfer of data blocks having intervals as recited in claim 19, wherein said at least one dead cycle comprises N - M dead cycles.

21. (Original) The method for effectuating the transfer of data blocks having intervals as recited in claim 19, wherein the operation of receiving packet data and advance notice further comprises receiving advance notice indicative of the location of at least one dead cycle 0 to N - 1 cycles prior to the location of said dead cycle.

22. (Original) The method for effectuating the transfer of data blocks having intervals as recited in claim 19, wherein the operation of transmitting ordered contiguous data blocks about said dead cycle further comprises transmitting at least one of said data blocks adjacent to said dead cycle.

23. (Currently Amended) A computer system having circuitry for effectuating the transfer of data blocks having intervals across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second clock signal (CLK2), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

means for generating advance notice indicative of the location of at least one dead cycle occurring between a first clock signal and a second clock signal used for transmitting data across a clock boundary;

means for receiving packet data and said advance notice indicative of the location of said at least one dead cycle, said packet data including said data blocks having intervals;

means for calculating the optimal time to send said packet data relative to the location of said at least one dead cycle; and

means for transmitting ordered contiguous data blocks about said at least one dead cycle to a CLK1-to-CLK2 synchronizer for

transmission to receive circuitry disposed in said second clock domain.

24. (New) The computer system having circuitry for effectuating the transfer of data blocks having intervals as recited in claim 23, further comprising means for receiving and temporarily storing a first portion of said data blocks having intervals and means for selecting between said first portion of said data blocks and a second portion of said data blocks having intervals provided without queuing.